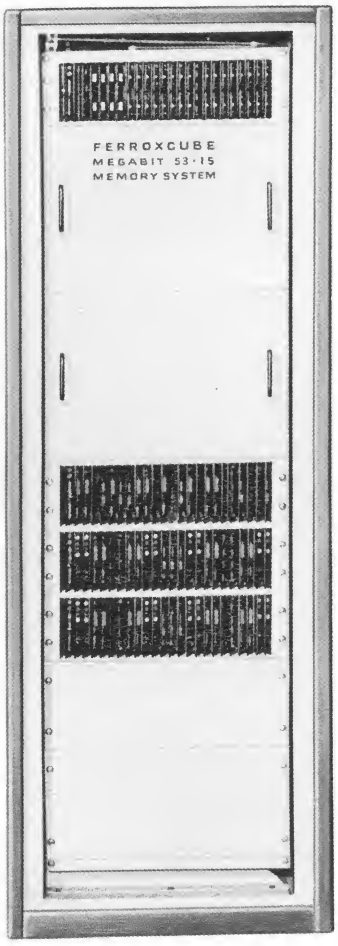
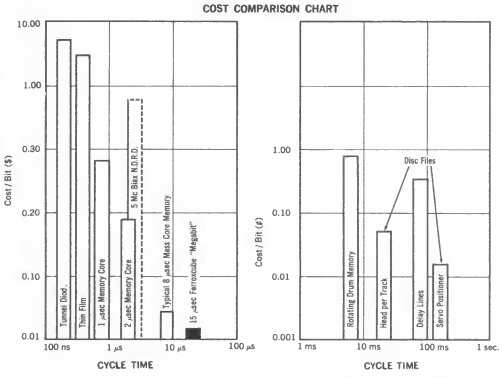
FERROXCUBE 15 MICROSECOND MASS MEMORY SYSTEMS



STANDARD 53.15 RANDOM ACCESS, MAGNETIC CORE MEMORY —15 USEC CYCLE TIME



Here are per bit costs on ten existing memory devices. For the first time, a ferrite memory system, Megabit 53.15 competes most favorably with devices that are not truly random access.

Available today in a 65K (76 bit) configuration, the new Ferroxcube Standard "Megabit" 53.15 is priced at only 1¾¢ per bit, or an average of $87,500 per system. This low cost, truly random access system will offer even lower prices per bit as the line develops.

Megabit 53.15 offers both computer manufacturers and users alike, a full complement of features. Designed with applications in mind, the "immediately useful" 5 million bit size can be expanded whenever desired by adding on additional 5 million bit modules. For existing systems, Megabit 53.15 can cut sorting and merging time by one third thereby releasing vital computation time and extending any system's efficiency.

Combining this new low price with random access, you can now economically extend main memory rather than using equipment that is not truly random access such as disc or drum devices.

Only 25" x 26" x 76", Megabit 53.15 is a compact, compatible system which integrates power supply, standard memory exerciser, and memory retention unit.

The Megabit 53.15 Memory System is an outgrowth of Ferroxcube's 15 years of experience in the design and manufacture of memory and switch cores, planes and stacks. All Ferroxcube memory systems are backed by highly trained Factory and Field Service Departments.

APPLICATIONS

In addition to providing new techniques for sorting and merging, Standard Megabit 53.15 Memory Systems offer new solutions for data retrieval and data handling. This new system is finding wide acceptance in commercial data processing, experimental, scientific, private and governmental laboratories and complex process control applications.

CIRCUIT FEATURES

MODES OF OPERATION

Read/Restore: Information stored at a particular address is read out, transferred to the computer or associated equipment, then rewritten at the same address.

Clear/Write: Information stored at a particular address is erased and new information is written into this address.

Split Cycle: Information stored at a particular address is read out. At some later time, upon command, the write operation will write new information into this address. The write cycle, in this mode of operation, cannot be delayed by more than a 23 microsecond time span between read and write.

WORD SELECT MEMORY CORE STACK

This Ferroxcube Memory Stack is organized as a word-select system. Selection is accomplished with switch cores, which are in turn, selected in a coincident current method. In the word select memory stack only one wire is effectively used for both sensing and inhibiting . . . a major contribution to the ultimate low cost of this unit.

SWITCH CORE MATRIX

The switch core matrix is used to select and drive the elements in the memory stack array. A wire looped through each switch core is, in effect, the linear select wire for the cores in the memory array.

LOGIC CIRCUITRY

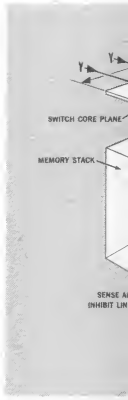
Logic circuit modules, employing silicon semiconductors, are potted and hermetically sealed. All modules are tested to ensure reliability under adverse temperatures, corrosion, salt spray, moisture, vibration and shock.

BASIC SYSTEM COMPONENTS

Memory Core Array
Switch Core Matrix
Input/Output Data Register
Timing & Control Unit
Memory Retention Unit
(ONE's and ZERO's only)
Positive & Negative Selection Switches
Sense Amplifiers
Current Generator
Power Supplies
Memory Exerciser
Address Register
Inhibit Drivers

SYSTEM SPECIFICATIONS

CYCLE TIME:	15 microseconds
ACCESS TIME:	2 microseconds or less
CAPACITY:	65K x 76
TEMPERATURE:	10°C to 40°C
INPUT/OUTPUT LEVELS:	Silicon logic: Logic "0" = +6 volts. Logic "1" = 0 volts. Can be supplied to meet other equipment requirements.
POWER:	115 volts, 60 cps
PHYSICAL DIMENSIONS:	25" wide by 26" deep by 76" high — AN EXTREMELY SMALL UNIT FOR A CAPACITY OF 65K x 76.



Switch cores
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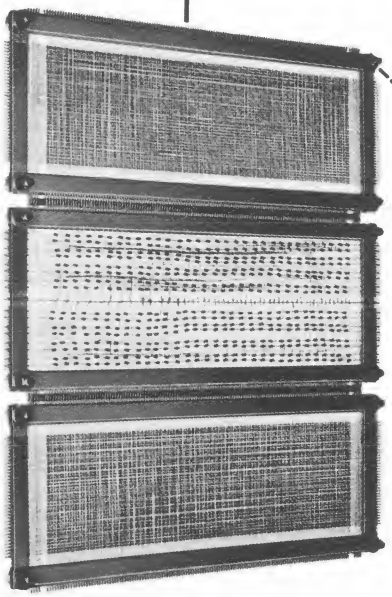
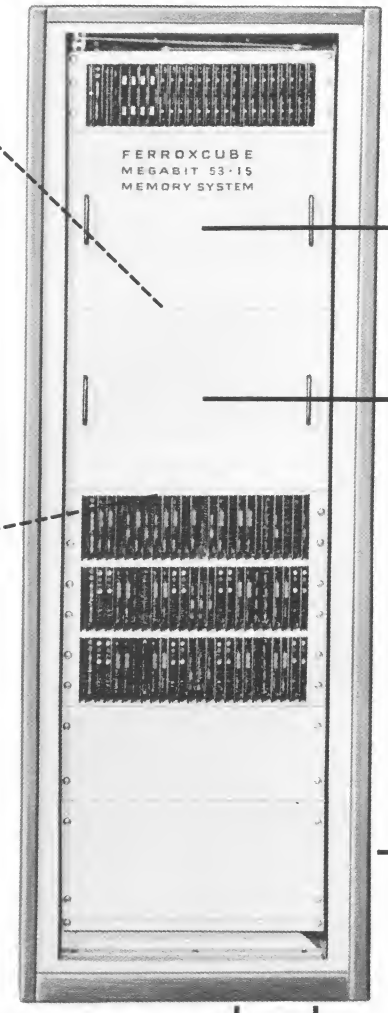
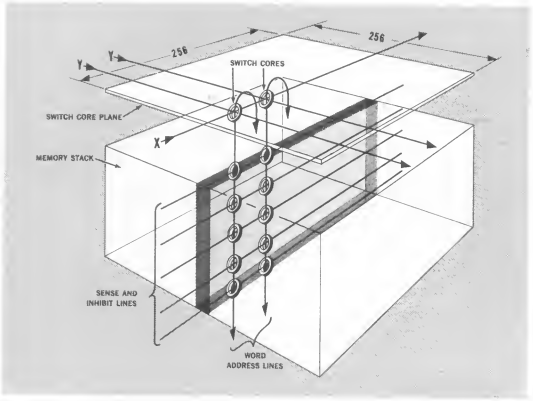






Megabit 53.15 **Memory and Switch Core Array**

Switch cores select the proper word line in a word-address stack array. Diagram illustrates how one wire can be utilized for both sense and inhibit functions. This is one of the key low cost features of the system. Only in the switch core array is a true coincident current selection approach used.

FEATURING...

Long Term Reliability — Application proven switch core matrix reduces diode and semi-conductor requirements by 30%. This means simpler, uncompromised design to use . . . a smaller more reliable unit to you. Ferroxcube cores assure exceptional temperature stability and coupled with hermetically sealed modules, provide excellent overall environmental stability.

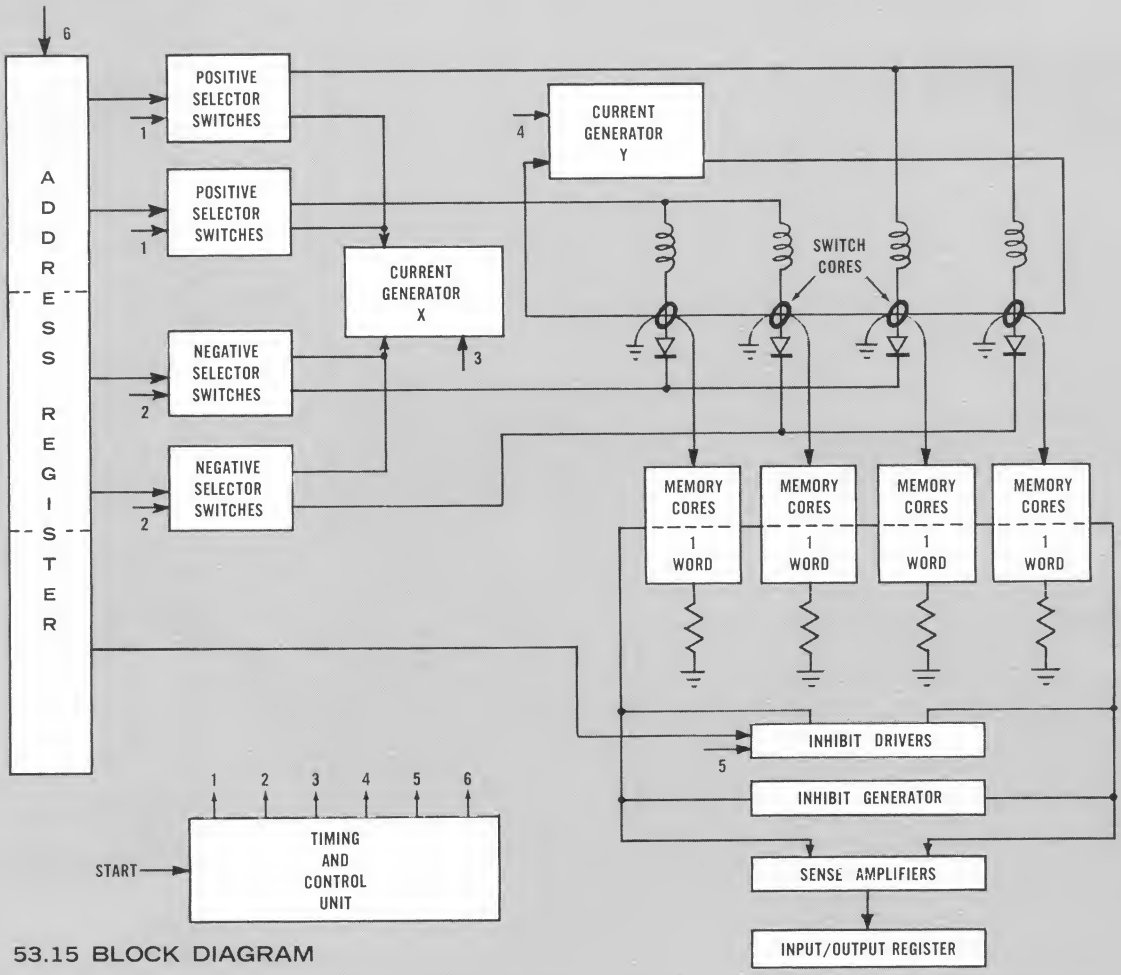
Large Storage Capacity — Basic configuration of 65K x 76. The computer manufacturer can now purchase additional 5-million bit modules . . . use complete capacity immediately.

True Random Access Memory — Unlike discs and drum memories, the Megabit 53.15 has the ability to provide access to any information in storage within the same constant time frame.

No Investment Costs — Here's a case where you can specify standard memory at only 1¾¢ per bit . . . with no investment on your part. And with the long standing ferrite memory device experience at Ferroxcube, you need not worry or commit unnecessary dollars to state-of-the-art core or film development.

Small Compatible Size — Physical dimensions are only 25" x 26" x 76", including power supply, standard memory exerciser and standard memory retention unit. Nowhere in industry can you purchase mass memory of this type in this compact size.

Standard Memory Retention Unit and Memory Exerciser — All Ferroxcube Megabit 53.15 Systems have these two critical units built-in at no extra cost. Retention unit guards against lost data and programs due to power failures. Exerciser permits quick testing of memory . . . quickly spots any memory failure.



53.15 BLOCK DIAGRAM

DESIGN CONSIDERATIONS

Demand for an extremely low price per bit by computer manufacturers and end users places severe design requirements on any memory core stack array. Since the memory stack is by far the most critical and expensive component of the memory, Ferroxcube designed the 53.15 stack as a word address system. To employ as few selection switches as possible, selection takes place through a switch core matrix. The switch cores, in turn, are coincident current selected. To maintain simple design within the stack itself, the same wire is used for both sense and inhibit.

This minimum configuration contains 256 x 256 words, each word driven by one switch core. Therefore, there are an equal number of switch cores — one on each intersection of 256 "X" drive wires and 256 "Y" drive wires. All switch cores are threaded by a third wire carrying a bias current. Finally, each switch core is threaded by a fourth wire which couples the switch core to the 76 memory cores of one word. One switch core, and thereby one word, is isolated by selecting one out of the 256 "X" wires and one out of the 256 "Y" wires.

To reduce the number of selection switches, group selection principles are used. The 256 drive wires of one coordinate are connected in 16 groups, each group terminating in a selection switch. The same technique is used on the opposite side of the stack array, again terminating in a selection switch. The current generator is connected between the selection switches on both sides of the stack.

Employing one wire for both sense and inhibit places tight design requirements on the read amplifier. This amplifier must recover from the inhibit noise quickly enough to detect a ZERO or ONE output micro-seconds later. This recovery time, not only in the read amplifier but also in the stack allows for decaying transients and is one of the main parameters governing cycle time.

To avoid extreme over-drive of the read amplifier, Ferroxcube designers intersect the bit wire in four identical parts. These four sections are then connected in a bridge circuit which is driven by the inhibit source across one diagonal and sensed by the read amplifier across the other diagonal. To accomplish this in the actual unit, the memory array is constructed of four independent modules. Each module contains one fourth the 65K and 76 capacity. The common sense and inhibit wire from each module is connected to the four respective corners of the balanced bridge.

The Megabit 53.15 has been designed by memory people for the computer industry with end use in mind. Application abilities have not been compromised with cost. Engineering technique has not been sacrificed for expediency. You can specify Megabit 53.15 — and gain the competitive edge.

Warranty and Field Service — Material and workmanship in each Ferroxcube Megabit 53.15 Memory System is warranted for one year from date of delivery. Any service required during this warranty period will be performed, upon customer request, by the Ferroxcube Field Engineering Department.

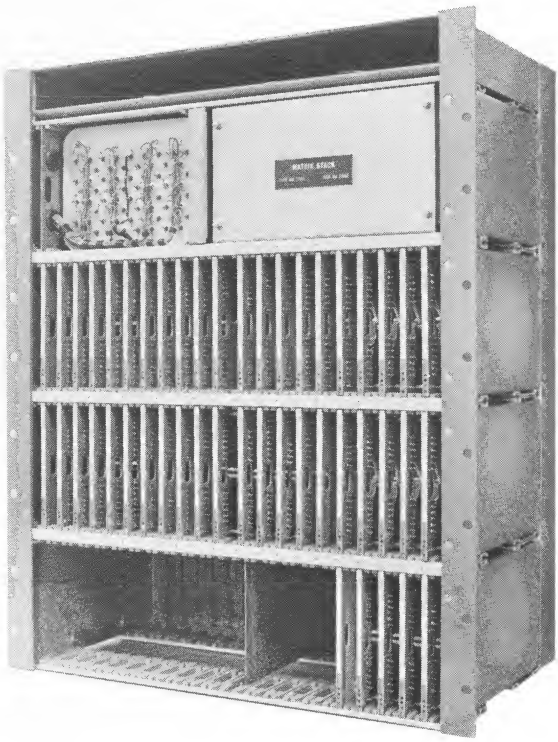
Ordering Information — the Megabit 53.15 Memory System meets many specific applications. Let us know your requirement for capacity, operating mode and input-output specifications. Our Application Engineering Department will work closely with you. Phone 914-246-2812, Saugerties, New York.

FERROXCUBE CORPORATION OF AMERICA/SAUGERTIES, N.Y.

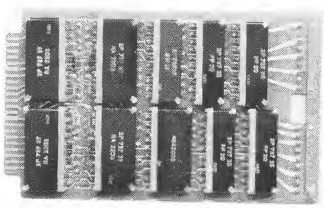
7.5M (5/65) 1804A

Printed in U.S.A.

Ferroxcube Standard 2 Microsecond Memory Systems



Ferroxcube 52.02 Memory Systems are high speed units which provide read/write cycle times of 2 microseconds, access times of .9 microseconds or better, and industries highest operating margins of 5 to 8%. These systems, another extension in the expanding family of Ferroxcube Memory Systems, are designed on the random access, coincident current principal. Capacities run up to a maximum of 16,384 words of 26 bits each.



Silicon logic modules offer today's widest operating temperatures.

Temperature flexibility without ovens or controlled environment is a major advantage of this high speed line. You can specify the 52.02 WT group with a broader temperature range of 0-50°C, or the 52.02 group which offers a temperature range of 10-35°C. Both lines utilize complete silicon circuitry. All printed circuit connectors, cards, as well as interface plugs and connectors are manufactured to MIL standards. Of special importance is the optional memory retention control unit which gives fast a-c power fault recognition and interruption. With this control unit you no longer need to fear critical loss of stored information and unnecessary rewrite time.

Each Ferroxcube Memory System is backed by over a decade of ferrite technology, so that today Ferroxcube is a company capable of designing and manufacturing its own cores, planes, stacks and systems . . . **and this is the straight road to higher margins.**

APPLICATIONS

Standard Ferroxcube 52.02 WT Memory Systems are designed for those applications which put a premium on fast response. Two typical uses are in the computer industry and the telemetry or data acquisition fields. Each memory bank has its own input/output and address logic, providing an effective cycle time of one microsecond or less when multiplexing or parallel operation of the memory bank is utilized.

CIRCUIT FEATURES

ACCESS METHODS

Random (Standard): In a random access operation, the system permits storage and removal of information at random. In this method there is no restriction as to the order in which addresses may be selected, or the number of times a given address may be interrogated.

Sequential (Optional): In this method, the 52.02 accepts information in a prescribed manner during the write operation, and stores it in the memory in a sequential order, starting with the first address and proceeding to the next address in the address register. This procedure is followed until an entire prescribed sequence of addresses has been handled. To read, the address register is reset to the prescribed starting point, and the information is read in the order in which it was stored.

Sequential Interlace (Optional): As the name implies, this method is also a sequential operation. The difference between the sequential interlace and the sequential non-interlace is the use of a second address register that permits information to be loaded and unloaded in independent sequence. The last storage information location for either write or read is retained in each respective address register.

MODES OF OPERATION

FULL CYCLE

Read/Restore: Information stored at a particular address is read out, transferred to the computer or associated equipment, and then rewritten at the same address.

Clear/Write: Information stored at a particular address is erased and new information is written into this address.

SPLIT CYCLE

Information stored at a particular address is read out. At some later time, upon command, the write operation will write new information into this address. The overall read/write cycle time is dependent solely upon the time between read and write commands.

300% MEMORY ELEMENT TEST

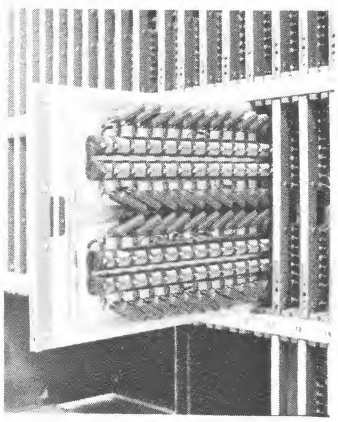
Ferroxcube assures maximum reliability by 300% testing of all memory elements. Each core 100% tested at manufacturing stage, 100% tested after assembly in the plane, and 100% tested after planes are assembled into a stack. All tests are conducted to narrow-range specifications on all electrical parameters.

BASIC SYSTEM COMPONENTS

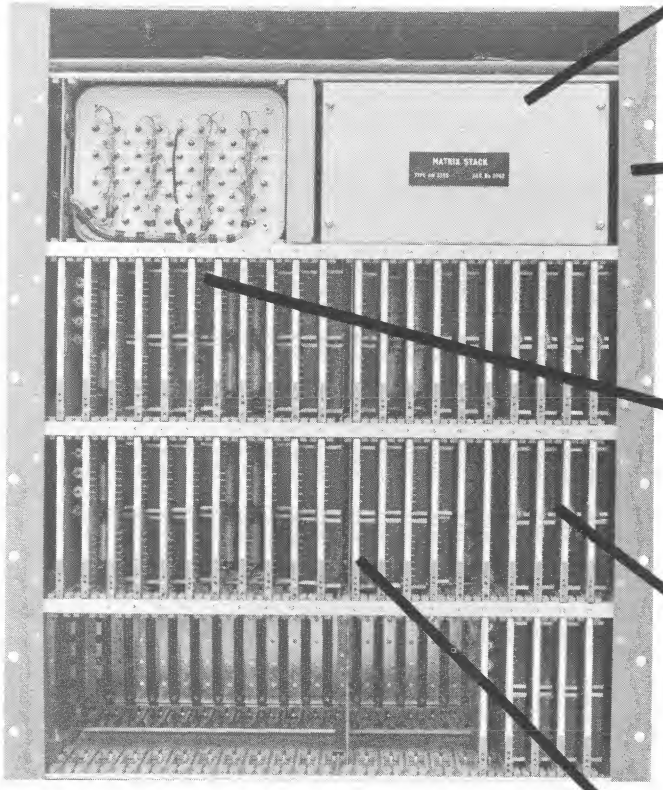
Memory Core Array
Transformer Selection Matrix
Address Register & Decoding Circuit
Input/Output Data Register
Timing & Control Unit
Inhibit Current Drivers
X & Y Current Drivers
Sense Amplifiers
Power Supplies

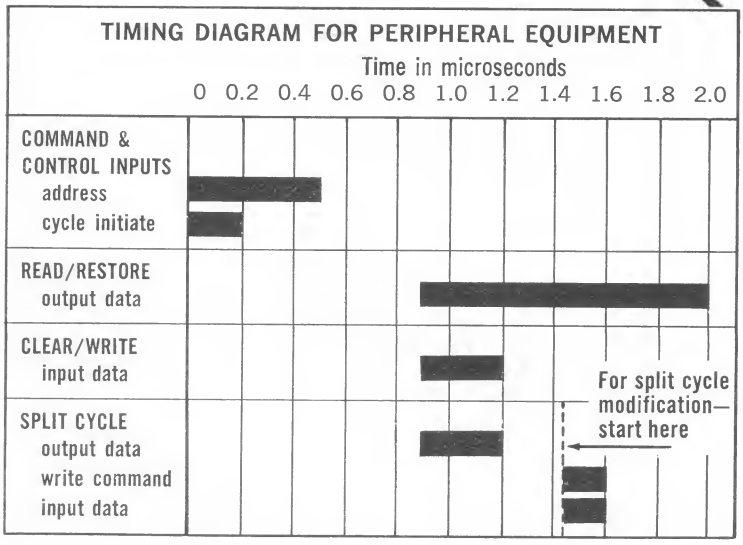
SYSTEM SPECIFICATIONS

CYCLE TIME:	Full 2 microseconds.
ACCESS TIME:	Less than 1 microsecond.
CAPACITY:	16,384 words maximum, in bit lengths to 26 to meet application requirements.
INPUT/OUTPUT LEVELS:	Silicon logic = +6 and 0 volts. Can also be supplied to meet other customer requirements.
TEMPERATURE:	52.02 WT — 0-50°C without ovens or controlled environments. 52.02 — 10-35°C without ovens or controlled environments.
POWER:	115 VAC, 60 cps.
PHYSICAL DIMENSIONS:	Fits all standard 19″ EIA relay rack channels. Height depends on system capacity. Typical 4096 x 32 unit (without power supplier) measures only 19″W x 23″H x 10¾″D.



Accurate Internal Delay Line Timing — Assures that memory timing does not vary if system parameters fluctuate. Cycle and access times never change.





FEATURING...

Widest Operating Margins — a healthy 5-8%. Now current can vary up to four times as much as nearest competitive system. Ferroxcube 52.02 WT and 52.02 systems also feature automatic current compensation of the power supplies.

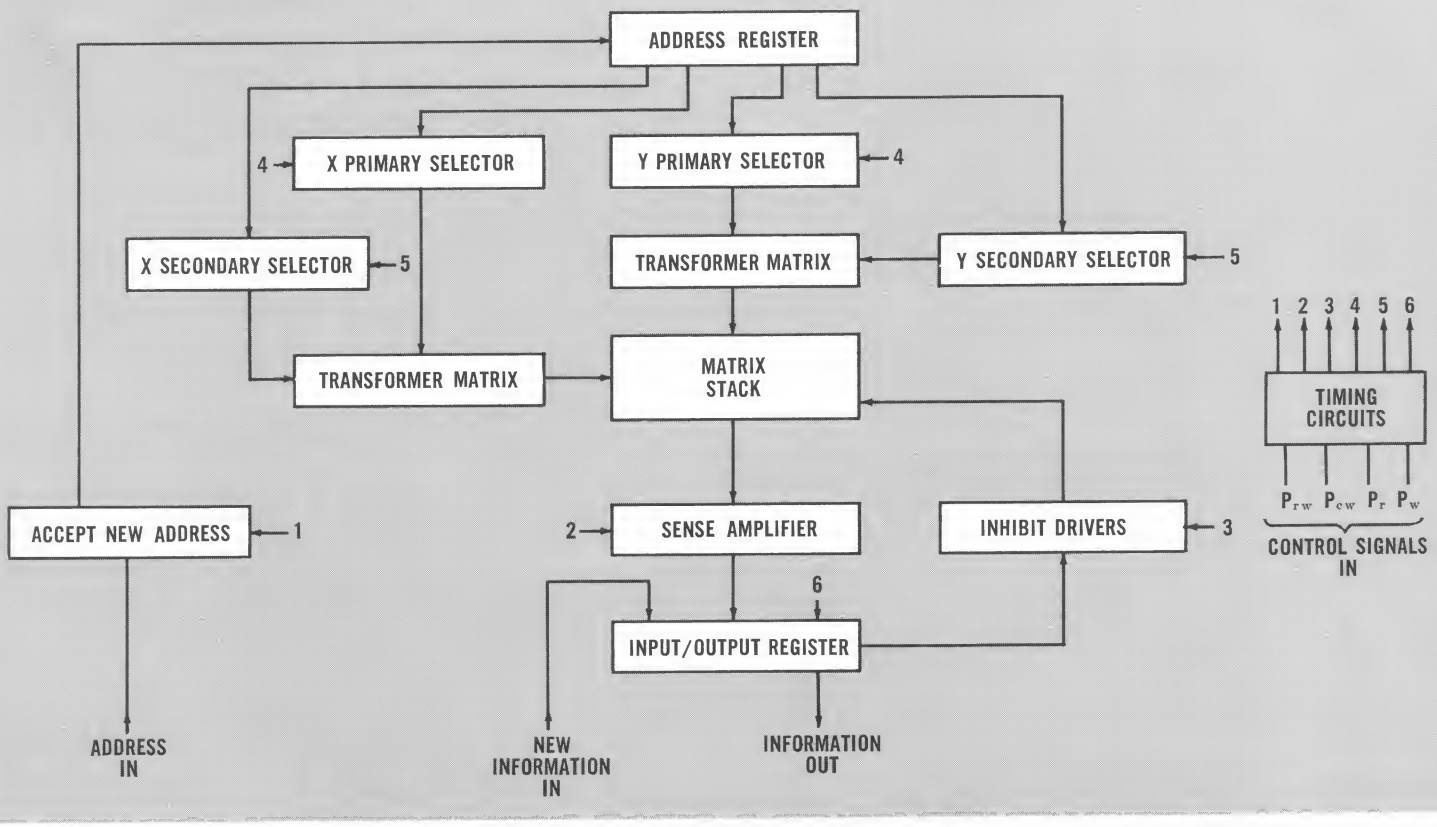
Standard Systems — means fast delivery, lower cost, and many different configurations. By offering proven design in quantity, Ferroxcube is uniquely capable of offering a new level of memory system reliability.

Versatile Input/Output Selection — as another standard feature, the Ferroxcube 52.02 WT and 52.02 provide up to 15-milliamp output current. Required current input is only 2 milliamps. As an optional feature, line drivers can be supplied to furnish 80 milliamps into a 75 ohm terminated, unbalanced tranmission line. Both standard and optional outputs give you more design flexibility.

Compact Over-all Dimensions — are only 19″W x 23″H x 10¾″D (without power supply) for a typical 4K x 32 rack mounted unit. Increasing the capacity to 16,384 words, 26 bits long, increases the height by only 9″.

Solid State Circuit Modules — insure maximum reliability over entire temperature range. Basic logic circuit is a 2 MC diode-transistor NAND circuit. Modules are mounted on plug-in printed circuit cards with convenient test points for trouble shooting. Blocks are given strict environmental tests — moisture, vibration, shock, temperature and corrosion.

52.02 WT / 52.02 BLOCK DIAGRAM



PRINCIPLES OF OPERATION

Address information from the computer or interfaced device is transferred into the memory address register. This information is decoded to select one transformer in the X transformer matrix and one transformer in the Y transformer matrix.

Command information as to the type of cycle to be performed is accepted by the timing and control unit which stores the command and initiates the proper sequence of timings.

The read timing is gated with the decoded read selection switches and drivers which direct a read current through the selected transformers. The transformers each provide a half select read current down the drive lines. The coincidence of currents in the core stack (one from the selected X-drive line transformer and one from the selected Y-drive line transformer) reads out the desired word from the stack. The word read out is detected by the sense amplifiers and if a read cycle is being performed, it is transferred to the input-output register and from there, to the computer or other external device.

To perform the write or restore portion of the cycle, the write timing from the control unit is gated with the decoded write selection switches and drivers and a current opposite to the read is directed to the drive lines via the selected transformers. Coincidence of X and Y drive write currents in the core stack attempt to set all bits of the selected word to 'one'. At the same time, the timing is gated with the input-output register data to turn on the inhibit drivers for those bits being written which are to be 'zero'. This inhibit current prevents the core from being switched.

To perform a write cycle, the information read out of the stack into the sense amplifier is not gated to the input-output registers and the new information which is gated into the input-output register from the computer controls the digit drivers and is written into the cleared address during the write portion of the cycle.

To perform a split cycle, the information read out of the stack during the read portion is gated from the sense amplifiers to the input-output register and out to the computer. The input-output register is cleared to prepare it to accept new information. The timing unit does not start the write portion of the cycle, but waits until new data has been transferred into the input-output register from the computer. On command from the computer, the timing unit will then initiate the write portion of the cycle.

The split cycle provides the means to read a word out of the memory, edit or alter it, and restore it to its original location.

WARRANTY AND FIELD SERVICE — Material and workmanship in each Ferroxcube Memory System is warranted for 1 year from the date of delivery. Any service required during this warranty period will be performed, upon customer request, by the Ferroxcube Field Engineering Department.

ORDERING INFORMATION — The 52.02WT and 52.02 Memory Systems thru a high degree of system flexibility, are adaptable to many specific applications. Consult with us regarding your requirements for capacity, operating modes, and input/output specifications. Our Application Engineering Department will be happy to work with you on your specific memory requirements. Phone 914-246-2811, Saugerties, N. Y.